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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech I Year II Semester Regular Examinations May 2019

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours

Max. Marks: 60

PART-A

(Answer all the Questions 5 x 2 = 10 Marks)

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|---|---|--|----|
| 1 | a | Convert (15) ₁₀ to Binary | 2M |
| | b | Define Pair, Quad, and Octet | 2M |
| | c | Construct 2:1 multiplexer. | 2M |
| | d | Difference between latch and flip-flop | 2M |
| | e | Define the Static RAM and Dynamic RAM | 2M |

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

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|---|---|--|----|
| 2 | a | Convert the following numbers
i)(163.789) ₁₀ to Octal number ii)(11001101.0101) ₂ to base-8 and base-4
iii)(4567) ₁₀ to base2 iv) (4D.56) ₁₆ to Binary | 5M |
| | b | Subtract (111001) ₂ from (101011) using 1's complement? | 5M |

OR

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| 3 | Explain the Binary codes with examples. | 10M |
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UNIT-II

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| 4 | Simplify the Boolean expression using K-MAP
$F(A,B,C,D,E) = \sum m(0,1,4,5,16,17,21,25,29)$ | 10M |
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OR

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| 5 | Reduce the expression $f(x,y,z,w) = \pi M(0,2,7,8,9,10,11,15)$.d (3,4) using K-Map. | 10M |
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UNIT-III

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| 6 | Implement BCD to 7-segment decoder for cathode type using 4:16 decoder. | 10M |
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OR

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| 7 | Design the combinational circuit binary to gray code. | 10M |
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UNIT-IV

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| 8 | a | Draw and explain the operation of D Flip-Flop. | 6M |
| | b | Explain about Shift Registers. | 4M |

OR

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| 9 | a | Explain about ripple counter. | 5M |
| | b | What is state assignment? Explain with a suitable example. | 5M |

UNIT-V

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| 10 | Write about the following.
i) Transistor-transistor Logic (TTL)
ii) Emitter – coupled Logic (ECL)
iii) CMOS Logic | 10M |
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OR

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| 11 | Implement the following functions using PLA.
$A(x,y,z) = \sum m(1,2,4,6)$ $B(x,y,z) = \sum m(0,1,6,7)$ $c(x,y,z) = \sum m(2,6)$ | 10M |
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END